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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,146	04/14/2004	Daniel James Winarski	TUC920040008US1	7829

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EXAMINER

KROFCHECK, MICHAEL C

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/825,146

Applicant(s)

WINARSKI ET AL.

Examiner

Michael Krofcheck

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-9 and 11-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-9 and 11-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the amendment filed on 9/27/2006.
2. The abstract, specification, and claims 1, 8, and 16 have been amended.
3. Claims 3, 10, and 18 have been cancelled.
4. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-9, 11-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
7. Claim 8 recites the limitation "said write command" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

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9. Claims 16-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

10. Claims 16-17 are not limited to tangible embodiments. In view of the applicant's disclosure, specification page 18, paragraph 0035, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., volatile and non-volatile memory) and intangible embodiments (e.g., signals propagating through space, radio waves, infrared signals). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

The examiner recommends that the applicant amend the claim to state, "An article of manufacture comprising a **computer readable** data storage medium..." since paragraph 0035 of the definition in the specification of computer readable medium article of manufacture is limited to tangible embodiments, while the transmission media article of manufacture contains intangible embodiments.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 1, 2, 7-9, 11, 12, 16, 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis et al., US patent 5233576, Takahashi, US patent 6373800, Debiez et al., US patent application publication 2003/0126359, and Morgan, III US patent application publication 2003/0033316.

15. With respect to claim 1 and 16, Curtis teaches of a method for writing data on data storage media in a data storage device, comprising: said data storage device receiving a write command (fig. 1; column 4, lines 59-61, column 4, line 68-column 5, line 7; as the processor transfers data to the data storage device, it is abundantly clear to one of ordinary skill in the art that it involves a write command);

obtaining a LBA WORM utilization bit from a WORM memory for each of said one or more destination LBAs (fig. 6; column 6, line 66-column 7, line 3); and

in response to said LBA WORM utilization bit indicating a rewriteable LBA for each of said one or more destination LBAs, executing said write command to write data to said one or more destination LBAs (fig. 6; item 608, 610 column 7, lines 3-7)

an article of manufacture comprising a data storage medium tangibly embodying a program of machine-readable instruction executable by a digital processing apparatus to perform the method steps (fig. 1; column 5, lines 4-7).

Curtis fails to explicitly teach of obtaining a starting LBA and a LBA transfer length from said write command; using said starting LBA and said LBA transfer length to determine one or more destination LBAs for writing data to.

However, Takahashi teaches of obtaining a starting LBA and a LBA transfer length from said write command (column 9, lines 45-51);

using said starting LBA and said LBA transfer length to determine one or more destination LBAs for writing data to (column 9, lines 45-51; the starting logic number sector and the number of blocks directly indicate the destination LBAs);

The combination of Curtis and Takahashi teaches of obtaining a WORM bit from said write command (Curtis, column 7, lines 17-24; it is abundantly clear to one of ordinary skill in the art to integrate the change-state of command with the write command to reduce the traffic over the system bus, and increase the processing efficiency); and

in response to determining that said write command executed without errors and that said WORM bit indicates WORM data, setting said LBA WORM utilization bit for said one or more destination LBAs in said WORM memory to indicate WORM data

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(Curtis, column 7, lines 17-24; it is abundantly clear to one of ordinary skill in the art to ensure that the writing has executed without errors before changing the state of the written data to read only, as if it were changed when there were errors, the result would be corrupted space on the storage device that is unusable).

The combination of Curtis and Takahashi fails to explicitly teach of said WORM memory is separate from said data media. However, Debiez teaches of an external WORM module that stores the block number of blocks that are not to be over written (fig. 1; paragraph 0011; as the block numbers stored it is abundantly clear that there is a memory in the WORM module storing them).

The combination of Curtis, Takahashi, and Debiez fails to explicitly teach of wherein said WORM memory comprises one of an EPROM, a PROM, or a FLASH memory. However, Morgan teaches of static modifiable and non-modifiable storage devices such as a PROM or EPROM (paragraph 0057).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis and Takahashi at the time of the invention to use the write command contents of Takahashi in Curtis. Their motivation would have been to allow the processor to organize the data being written to the media by specifying its location; this helps to efficiently store the data.

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi and Debiez at the time of the invention to locate the storage state bits of the combination of Curtis and Takahashi in the WORM module of Debiez. By locating the storage state bits of Curtis in the WORM module of Debiez, the data

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protection is no longer reliant on the compatibility of the drive and can be accessed faster, reducing the time to access the storage media (Debiez, paragraph 0008).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi, Debiez and Morgan at the time of the invention to have the storage state bits in the combination of Curtis, Takahashi, and Debiez stored in a PROM or EPROM taught by Morgan. Debiez expresses that it is not possible to overwrite the block number stored in the WORM module, storing the block numbers in a PROM as taught in Morgan would prohibit them from being overwritten as will storing them in an EPROM. EPROM are completely erased only by removing the chip from the circuit, removing the tape from the chip and exposing it to an intense UV light for 20 minutes. As there is no other way to modify an EPROM, the data within can't be modified by the computer it is located in.

16. With respect to claim 8, the combination of Curtis, Takahashi, Debiez and Morgan teach of the limitations of claim 8 that are recited above with respect to claims 1 and 16.

In addition, Curtis teaches of a processor for controlling said data storage device (fig. 1; item 124; column 5, lines 4-7; the controller must contain a processor);

a WORM memory coupled to said processor for storage of a LBA WORM utilization bit (fig. 1, 2; item 126, 200; column 4, lines 40-49; as when the storage bit is set, it cannot be changed, it is stored in a WORM);

a host device interface coupled to said processor for receiving commands from a host computer (fig. 1; item 122; column 4, line 56-column 5, line 4).

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17. With respect to claims 2 and 17, Curtis teaches of in response to said LBA WORM utilization bit indicating a WORM LBA for any of said one or more destination LBAs, not executing said write command (fig. 6; item 608; column 7, lines 4-5).

18. With respect to claim 7, Curtis teaches of wherein said write command writes said data as WORM data on said data storage device (column 7, lines 5-24; where the data is written into the sector and the state of the sector is changed to read-only).

19. With respect to claim 9, Curtis teaches of wherein said data is stored as WORM data on said data storage media (column 7, lines 5-24; where the data is written into the sector and the state of the sector is changed to read-only).

20. With respect to claims 11 and 12, the combination of Curtis, Takahashi, Debiez and Morgan, specifically, Morgan teaches of the limitations of claims 11 and 12 as cited above with respect to claims 1 and 16.

21. Claim 4-6 rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis Takahashi, Debiez and Morgan as applied to claim 1 above, and further in view of Assouad, US patent 6084739.

22. With respect to claims 4 and 5, the combination of Curtis, Takahashi, Debiez and Morgan fails to explicitly teach of in response to determining that said write command executed with at least one error, rewriting the data beginning at said starting LBA.

However, Assouad teaches of in response to determining that said write command executed with at least one error, rewriting the data beginning at said starting LBA (fig. 7; column 6, lines 53-67; the write operation is retried at the targeted address, when an error occurs).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi, Debiez, Morgan, and Assouad at the time of the invention to retry the write operation at the target address upon the occurrence of an error in the combination of Curtis, Takahashi, Debiez, and Morgan as taught in Assouad. Their motivation would have been to ensure that the proper data is efficiently stored in the storage device without having to restart the writing process over again.

23. With respect to claim 6, the combination of Curtis, Takahashi, Debiez, Morgan, and Assouad teaches of in response to determining that said write command executed with at least one error, rewriting said data beginning at a LBA that is greater than said starting LBA (it is abundantly clear to one of ordinary skill in the art that when an error keeps occurring in a write operation, that the desired location maybe corrupt and to store the data at a location following the corrupt location to continue carrying out the instructions).

24. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis, Takahashi, Debiez, and Morgan as applied to claim 8 above, and further in view of Mambakkam et al., US patent 6976623.

25. With respect to claim 13, the combination of Curtis, Takahashi, Debiez, and Morgan fails to explicitly teach of wherein said WORM memory is a flash memory. However, Mambakkam teaches of WORM flash memory (column 1, lines 60-65, column 3, lines 45-49).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi, Debiez, Morgan and Mambakkam at the time of the invention to

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locate the storage state bits of the combination of Curtis, Takahashi, Debiez, and Morgan in WORM flash memory. Debiez expresses that it is not possible to overwrite the block number stored in the WORM module, storing the block numbers in a WORM flash memory as taught in Mambakkam would prohibit them from being overwritten.

26. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis, Takahashi, Debiez, and Morgan as applied to claim 8 above, and further in view of Do et al., US patent application publication 2002/0136214.

With respect to claim 14, the combination of Curtis, Takahashi, Debiez, and Morgan fails to explicitly teach of said WORM memory is located inside a sealed portion of said data storage device. However, Do teaches of wherein said WORM memory is located inside a sealed portion of said data storage device (fig. 2; paragraph 0156).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi, Debiez, Morgan and Do at the time of the invention to include the data storage device of the combination of Curtis, Takahashi, Debiez, and Morgan in the tamper-proof enclosure of Do. Their motivation would have been to ensure the data within is kept secure and can alert the proper party if unauthorized access is attempted (Do, paragraph 0156).

27. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis, Takahashi, Debiez, and Morgan as applied to claim 8 above, and further in view of Debiez et al., US patent application publication 2003/0126446 (hereinafter Debiez 2).

28. With respect to claim 15, the combination of Curtis, Takahashi, Debiez, and Morgan fails to explicitly teach of wherein said WORM memory, further comprises: a

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memory device for storage of a date stamp associated with each said LBA WORM utilization bit. However, Debiez 2 teaches of wherein said WORM memory, further comprises: a memory device for storage of a date stamp associated with each said LBA WORM utilization bit (paragraph 0021; it is abundantly clear to one of ordinary skill in the art that the timestamps include a date value, otherwise the timestamps would not be useful in authenticating the data).

It would have been obvious to one of ordinary skill in the art having the teachings of Curtis, Takahashi, Debiez, Morgan and Debiez 2 at the time of the invention to timestamp the writes to the storage sectors of the combination of Curtis, Takahashi, Debiez, and Morgan as taught in Debiez 2. Their motivation would have been to provide data integrity and timestamp authenticity to the stored data (Debiez 2, paragraph 0025).

Response to Arguments

29. Applicant's arguments filed on 9/27/2006 have been fully considered but they are not persuasive.

30. Applicant's arguments with respect to independent claims 1, 8, and 16 have been considered but are moot in view of the new ground(s) of rejection.

31. Applicant argues with respect to the 101 rejection, that the claims as written produce a useful, concrete and tangible result. The examiner, would like to point out, that this is **not** the reasoning behind why claims 16 and 17 are being rejected under 35 USC 101. The applicant claims an article of manufacture. In the specification, this

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article of manufacture is defined as a code or logic implemented in (1) hardware logic, (2) a computer readable medium, or (3) transmission media. As described in the specification (paragraph 0035), the transmission media is not tangible. As a result the claims are not statutory because they are not limited to a tangible embodiment. If the applicant were to make it clear in the respective claims, that only instances 1 and 2 were being claimed and not instance 3, then the claims would be statutory. For further explanation see MPEP §2106.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael Krofcheck